CLAIMS:

1. A power amplifier comprising:

a transconductance stage that is operable to receive an input voltage signal and to produce an output current signal; and

a cascode stage communicatively coupled to the transconductance stage that is operable to receive the output current signal and to produce an output voltage signal based thereupon, the cascode stage including a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar junction transistor formed in parallel with the MOS transistor, a gate of the MOS transistor and a base of the parasitic bipolar junction transistor each available for voltage control.

2. The power amplifier or claim 1, further comprising:

a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor and to controllably bias the base of the corresponding parasitic bipolar junction transistor.

3. The power amplifier of claim 1, wherein:

the MOS transistor comprises an N type source and an N type drain formed in a P type substrate to define a channel there between and a gate formed upon the P type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P type substrate; and

further comprising a P+ base contact corresponding to the parasitic bipolar transistor formed in the P type substrate.

4. The power amplifier of claim 1, wherein:

the MOS transistor comprises a P type source and a P type drain formed in an N type substrate to define a channel there between and a gate formed upon the N type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact corresponding to the parasitic bipolar transistor formed in the N type substrate.

5. The power amplifier of claim 2, wherein the signal level detection and bias determination module is operable to apply a first bias voltage (V_{bc}) to the gate of the MOS transistor and to apply a second bias voltage (VB) to the base of the corresponding parasitic bipolar junction transistor.

6. The power amplifier of claim 1, wherein:

the transconductance stage comprises a transconductance element having a first terminal tied to ground and a second terminal;

the MOS transistor and the corresponding bipolar junction transistor include a shared first terminal and a shared second terminal coupled to the second terminal of the transconductance element; and

further comprising a circuit element coupled between a voltage supply and the shared first terminal of the MOS transistor and the corresponding bipolar junction transistor.

7. The power amplifier of claim 6, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

8. The power amplifier of claim 1, wherein:

the transconductance stage comprises a series combination of a transconductance element and a circuit element, the series combination coupled between a transconductance stage voltage supply and ground;

the cascode stage comprises:

a first circuit element having a first terminal coupled to ground and a second terminal;

a second circuit element having a first terminal tied to a cascode stage voltage supply and a second terminal;

a shared source/emitter terminal of the MOS transistor and the corresponding bipolar junction transistor coupled to the second terminal of the first circuit element and a shared drain/collector terminal of the MOS transistor and the corresponding bipolar junction transistor coupled to the second terminal of the second circuit element; and

an AC coupling stage that couples the output current signal produced by the transconductance stage to the cascode stage.

9. The power amplifier of claim 8, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

10. The power amplifier of claim 2, wherein the signal level detection and bias determination module is operable to turn off the MOS transistor and to controllably bias the corresponding parasitic bipolar junction transistor in an active range.

11. The power amplifier of claim 2, wherein the signal level detection and bias determination module is operable to turn off the corresponding parasitic bipolar junction transistor and to controllably bias the MOS transistor in an active range.

12. The power amplifier of claim 2, wherein the signal level detection and bias determination module is operable to controllably bias both the MOS transistor and the corresponding parasitic bipolar junction transistor in their active ranges.

13. A power amplifier comprising:

a transconductance stage coupled on a first side to ground and having a transconductance element, the transconductance stage operable to receive an input voltage signal and to produce an output current signal;

a cascode stage communicatively coupled on a first side to the transconductance stage and operable to receive the output current signal and to produce an output voltage signal based thereupon, the cascode stage including a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar junction transistor formed in parallel therewith, a gate of the MOS transistor and a base of the parasitic bipolar junction transistor each available for voltage control; and

at least one circuit element coupled between the cascode stage and a voltage supply.

14. The power amplifier of claim 13, further comprising a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor and to controllably bias the base of the corresponding parasitic bipolar junction transistor.

15. The power amplifier of claim 13, wherein:

the MOS transistor comprises an N type source and an N type drain formed in a P type substrate to define a channel there between and a gate formed upon the P type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P type substrate; and

further comprising a P+ base contact corresponding to the parasitic bipolar transistor formed in the P type substrate.

16. The power amplifier of claim 13, wherein:

the MOS transistor comprises a P type source and a P type drain formed in an N type substrate to define a channel there between and a gate formed upon the N type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact corresponding to the parasitic bipolar transistor formed in the N type substrate.

17. The power amplifier of claim 14, wherein the signal level detection and bias determination module is operable to apply a first bias voltage (Vbias) to the gate of the MOS transistor and to apply a second bias voltage (VB) to the base of the corresponding parasitic bipolar junction transistor.

18. The power amplifier of claim 13, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

19. The power amplifier of claim 14, wherein the signal level detection and bias determination module is operable to turn off the MOS transistor and to controllably bias the corresponding parasitic bipolar junction transistor in an active range.

20. The power amplifier of claim 14, wherein the signal level detection and bias determination module is operable to turn off the corresponding parasitic bipolar junction transistor and to controllably bias the MOS transistor in an active range.

21. The power amplifier of claim 14, wherein the signal level detection and bias determination module is operable to controllably bias both the MOS transistor and the corresponding parasitic bipolar junction transistor in their active ranges.

22. A power amplifier comprising:

a transconductance stage having a transconductance element and at least one circuit element and operable to receive an input voltage signal and to produce an output current signal;

an AC coupling stage communicatively coupled to the transconductance stage;

a cascode stage communicatively coupled to AC coupling stage to receive the output current signal thereby and to produce an output voltage signal based thereupon, the cascode stage including a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar junction transistor formed in parallel therewith, a gate of the MOS

transistor and a base of the parasitic bipolar junction transistor each available for voltage control, and at least one circuit element;

wherein the transconductance stage couples between a transconductance stage voltage supply and ground; and

wherein the cascode stage couples between a cascode stage voltage supply and ground.

23. The power amplifier of claim 22, further comprising a signal level detection and bias determination module operably coupled to the cascode stage that is operable to controllably bias the gate of the MOS transistor and to controllably bias the base of the corresponding parasitic bipolar junction transistor;

24. The power amplifier of claim 22, wherein:

the MOS transistor comprises an N type source and an N type drain formed in a P type substrate to define a channel there between and a gate formed upon the P type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the N type source, a collector corresponding to the N type drain, and a base corresponding to the P type substrate; and

further comprising a P+ base contact corresponding to the parasitic bipolar transistor formed in the P type substrate.

25. The power amplifier of claim 22, wherein:

the MOS transistor comprises a P type source and a P type drain formed in an N type substrate to define a channel there between and a gate formed upon the N type substrate above the channel;

the corresponding parasitic bipolar junction transistor comprises an emitter corresponding to the P type source, a collector corresponding to the P type drain, and a base corresponding to the N type substrate; and

further comprising a N+ base contact corresponding to the parasitic bipolar transistor formed in the N type substrate.

26. The power amplifier of claim 23, wherein the signal level detection and bias determination module is operable to apply a first bias voltage (Vbias) to a gate of the MOS transistor and to apply a second bias voltage (VB) to a base of the corresponding parasitic bipolar junction transistor.

27. The power amplifier of claim 23, wherein the transconductance element is selected from the group consisting of transistors and linearized transconductance stages.

28. The power amplifier of claim 23, wherein the signal level detection and bias determination module is operable to turn off the MOS transistor and to controllably biases the corresponding parasitic bipolar junction transistor in an active range.

29. The power amplifier of claim 23, wherein the signal level detection and bias determination module is operable to turn off the corresponding parasitic bipolar junction transistor and to controllably bias the MOS transistor in an active range.

30. The power amplifier of claim 23, wherein the signal level detection and bias determination module is operable to controllably bias both the MOS transistor and the corresponding parasitic bipolar junction transistor in their active ranges.

31. A method for amplifying a signal comprising:

receiving an input voltage signal;

producing an output current signal based upon the input voltage signal using a transconductance stage;

converting the output current signal to an output voltage signal using a cascode stage having a Metal Oxide Silicon (MOS) transistor and a corresponding parasitic bipolar junction transistor;

controllably biasing a gate of the MOS transistor; and

controllably biasing a base of the corresponding parasitic bipolar junction transistor.

32. The method of claim 31, wherein controllably biasing a gate of the MOS transistor and controllably biasing a base of the corresponding parasitic bipolar junction transistor comprises:

turning off the MOS transistor; and

controllably biasing the base of the corresponding parasitic bipolar junction transistor in an active range.

33. The method of claim 31, wherein controllably biasing a gate of the MOS transistor and controllably biasing a base of the corresponding parasitic bipolar junction transistor comprises:

turning off the corresponding parasitic bipolar junction transistor; and

controllably biasing the MOS transistor in an active range.

34. The method of claim 31, wherein controllably biasing a gate of the MOS transistor and controllably biasing a base of the corresponding parasitic bipolar junction transistor comprises biasing both the MOS transistor and the corresponding parasitic bipolar junction transistor in active ranges.